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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,784	03/22/1999	JOHN G. MCBRIDE	10971308-1	7570

22879 7590 01/15/2003

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EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/273,784	John McBride
Examiner	**Art Unit**
Thai Phan	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 8, 9, 15, and 16* is/are rejected.

7) ☒ Claim(s) *3-7, 10-14, and 17-20* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☒ Interview Summary (PTO-413) Paper No(s). 13
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

This Office Action is response to telephone interview with applicant's representative on Dec. 17, 2002. Due to typo error in the Office action, mailed on 11/04/2002, which cited cols. 9 and 10 on page 3, paragraph 1, does not exist in the reference, applicant's representative requested a new copy of Office action. Following is the Office action with corrected typo error.

Claim Rejections - 35 USC § 101

1. Applicant's arguments with respect to claim rejection under 35 USC 101 rejection is persuasive. The rejection is thus withdraw from this Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action.

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1, 2, 8, 9, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kochpatcharin et al., patent no. 5,844,818.

As per claims 1 and 15, Kochpatcharin anticipates method and system for design rule checking of an integrated circuit design with feature limitations as claimed (Abstract and Summary of the Invention). According to Kochpatcharin, the method and system for design rule checking includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 6, lines 19-51, for instance). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 4, line 5 to col. 6, line 60, for example), including checking noise susceptible or noise immunity as claimed for transistors to other transistors as claimed for design practice adherence or design quality as suggested use for in the Background of the Invention.

As per claim 2, Kochpatcharin anticipate reading transistor design parameters for design rule check as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics susceptible to noise in a specified design operation bound within thresholds values as known in MOS circuit operation (Background of the Invention).

As per claim 8, Kochpatcharin anticipates method for design rule checking of an integrated circuit design with feature limitations as claimed (Abstract and Summary of the

Invention). According to Kochpatcharin, the design rule checking method includes steps for receiving gate characteristics such as width and length of the design gate parameter for static gate rule checking, wherein the design gate usually contained more than one field effect transistor, and the gates connected in datapath or along circuit paths including static gate characteristics in which the gate characteristics involving with transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 6, lines 19-51, for instance). The rule checking method is to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-51, col. 6, lines 20-51), including checking noise susceptible or noise immunity as claimed for transistors to other transistors as claimed for design practice adherence or design quality as suggested in background of the invention.

As per claim 9, Kochpatcharin anticipate reading transistor design parameters for design rule check as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics susceptible to noise in a region of operation bound by threshold values as known in MOS device operation (Background of the Invention).

As per claim 16, Kochpatcharin anticipate reading transistor design parameters for design rule check as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule

checking of the gate circuit statically verifies device characteristics susceptible to noise, namely, within specific design threshold values as known in MOS circuit operation (Background of the Invention).

Allowable Subject Matter

4. Claims 3-7, 10-14, and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Dependent claims 3-7, 10-14, and 17-20 are objected to because the claims require a plurality of checking models for rule checking program and method, each rule checking model is associated with ratio of the width of the P-field transistor to the width of the N-field transistor, the ratio corresponding to the numerical value stored in the memory device. In each checking model, the rule checker program obtaining a (first) ratio of the width of the n and p-type transistor of the first model, the first ratio used to access the first and second threshold values stored in the memory device, the rule checker program determines noise levels on the inputs taking possible high or low values, and compares the determined noise levels to the first and second threshold values to determine the gate meets acceptable noise immunity requirement with respect to each model as claimed herein. The art of record does not expressly disclose such limitations as in the dependent claims.

Response to Arguments

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of a new ground of rejection.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

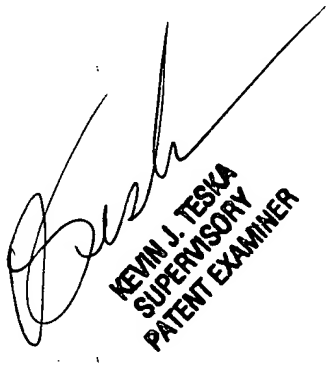
or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).



December 30, 2002